REMARKS/ARGUMENTS

Claims 1-16 remain in the application. Of these, claims 1-16 stand rejected.

1. Rejection of Claims 1-16 under 35 USC 112, Second Paragrph

Claims 1-16 stand rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1

The Examiner stated:

> As per claim 1, lines 2-4, "reading a test file including a plurality of test vectors...; and determining a required memory needed to execute the plurality of test vectors" is not clear how it determines a required memory needed to execute the test vectors, and it is also not clear how to execute the test vectors while the plurality of test vectors are reading out from the test file. Appropriate correction is required.

Claim 1 calls for a method comprising reading a test file including a plurality of test vectors to be applied to a device; and determining a required memory needed to execute the plurality of test vectors.

Applicant asserts that the limitation of "determining a required memory needed to execute the plurality of test vectors" clearly describes the subject matter of the present invention. The specification from paragraph [0016] through paragraph [0019] clearly describes the limitation of "determining a required memory needed to execute the plurality of test vectors" as follows:

> [0016] FIG. 3 illustrates an exemplary embodiment of a method for determining 205 a required memory. The method begins by determining 305 a first memory

requirement for a first pin to execute the test vectors for a first test in the test file. By way of example, the first memory requirement may be determined 305 by counting the number of test vectors in the first test for the first pin. The required memory is then set 310 to be equal to the first memory requirement.

[0017] Another pin of the tester having test vectors in the first test is selected and a second memory requirement for the selected pin to execute the test vectors for the first test is determined 315. The second memory requirement may be determined 315 by counting the number of test vectors in the first test for the selected pin. If the second memory requirement exceeds the current value of the required memory 320, the required memory is set 325 equal to the second memory requirement.

[0018] After 325, or if the second memory requirement does not exceed the current value of the required memory 320, a determination is made as to whether there are more pins 330 having test vectors in the first test to process. If there are more pins, processing continues back at 315 for the next pin. Otherwise, a determination is made as to whether there are more tests in the test file 335.

[0019] If there are more tests, 315-330 are repeated for the next test for each pin having test vectors to execute for the test. After all the tests have been processed, the method ends 340. Thus, it should be appreciated that at the conclusion of the method the required memory is determined to be equal to the memory requirements for the test and pin combination with the highest memory requirements.

Furthermore, the specification at paragraph also clearly describes the limitation of "determining a required memory needed to execute the plurality of test vectors" as follows:

[0020] In alternate embodiments, the required memory may be determined in a manner different from that shown in FIG. 3. The determination 205 may depend upon how available memory is allocated in the tester. For example, in one embodiment, the memory available for a pin may depend on the board where the pin is located. Pins on one board may have the same amount of memory available as other pins on the same board, while the amount of memory available for pins may vary between boards. In this embodiment, a required memory may be calculated for each board by determining the memory requirements for the test and pin combination with the highest memory requirements for each board using a method similar to that described in FIG. 3. In a second embodiment, memory may be allocated on a per pin basis. In this embodiment, a required memory may be determined for each pin. Other exemplary embodiments, such as embodiments with one memory available for all the pins of a board, may use corresponding different calculations.

Applicant respectfully requests clarification with respect to the Examiner's statement that "it is also not clear how to execute the test vectors while the plurality of test vectors are reading out from the test file". Applicant notes that claim 1 calls for a method comprising reading a test file including a plurality of test vectors to be applied to a device; and determining a required memory needed to execute the plurality of test vectors. There is no teaching "to execute the test vectors while the plurality of test vectors are reading out from the test file".

For at least the above-identified reasons, claim 1 is believed to be allowable.

Claims 2-9 and 16

The Examiner stated:

> As per claims 2-9, these claims are also rejected because they dependent upon the rejected base claim.

Applicant notes that claims 2-9, and also claim 16, each depend directly from independent claim 1. Claims 2-9 and 16 are each believed to be allowable for at least the same reasons identified above with respect to claim 1.

Claim 10

The Examiner stated:

> As per claim 10, lines 2-3, " logic to read a test file including a plurality of test vectors" is not clear how the logic determine a required memory needed to execute the plurality of test vectors and it is also unclear how the logic execute the plurality of test vectors while the plurality of test vectors are reading out from the test file? Appropriate correction is required.

Claim 10 calls for a system comprising logic to read a test file including a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors; and a tester, communicatively coupled to the logic, to apply the plurality of test vectors to a device.

Applicant asserts that the limitation of "logic to read a test file including a plurality of test vectors" clearly describes the subject matter of the present invention. The specification from paragraph [0012] through paragraph [0015] clearly describes the limitation of "logic to read a test file including a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors" as follows:

> [0012] The system also includes logic 160 communicatively coupled to tester 100. Logic 160 may be part of a test operating system on a workstation coupled to tester 100 via a communication link, such as an optical link. In one embodiment, logic 160 may communicate with firmware (not shown) on tester 100 to send tests to device 150 and receive test results. In an alternate embodiment, logic 160 may be part of the firmware of tester 100.
> [0013] As shown in FIG. 2, logic 160 may be used to read 200 a test file containing one or more tests to be performed on device 150. Each of the tests may include a plurality of test vectors to be applied to device 150. Logic 160 may then determine 205 a required memory needed to execute the plurality of test vectors. By way of example, the number of test vectors for each test in the test file may be counted and the required memory may be determined to be equal to the number of test vectors required for the test with the highest number of test vectors.
> [0014] The determination 205 may be performed before, during, or after, execution of the tests. If the determination is made before or during testing, a user may be notified of additional memory requirements or the memory may be dynamically increased as will be described below. In other embodiments, the maximum amount of memory may be made available to the tester and the memory calculation may be used to bill a customer after usage of the memory.
> [0015] Logic 160 may determine 205 a required memory needed for each board of a tester to execute the test vectors for the board. In embodiments having a memory associated with each pin, a required memory needed for each board may be determined by determining the memory requirements for the pin with the highest memory usage. Alternately or additionally, logic 150 may determine 205 the required memory needed for each pin to execute the vectors for the pin.

Applicant respectfully requests clarification with respect to the Examiner's statement that "it is also unclear how the logic execute the plurality of test vectors while the plurality of test vectors are reading out from the test file". Applicant notes that claim 10 calls for "a system comprising logic to read a test file including a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors; and a tester, communicatively coupled to the logic, to apply the plurality of test

vectors to a device." There is no teaching "execute the plurality of test vectors while the plurality of test vectors are reading out from the test file".

For at least the above-identified reasons, claim 10 is believed to be allowable.

Claims 11-15

The Examiner stated:

> As per claims 11-16, these claims are also rejected because they dependent upon the rejected base claim.

Applicants note that claims 11-15, but not claim 16, each depend directly from independent claim 1. Claim 16 depends directly from independent claim 1, and claim 16 is discussed above. Claims 11-15 are each believed to be allowable for at least the same reasons identified above with respect to claim 10.

2. Provisional Rejection of Claims 1-6 and 10-13 under the Judicially Created Doctrine of Obviousness-Type Double Patenting

Claims 1-6 and 10-13 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting, as being unpatentable over claims 1, 3-7, 13 and 17 of copending Application No. 10/681,068. The Examiner's rejection is duly noted, and a Terminal Disclaimer will be filed if and when Application No. 10/681,068 matures into a patent.

3. Rejection of Claims 1-16 under 35 USC 102(b)

Claims 1-16 stand rejected under 35 USC 102(b) as being anticipated by Regelman (US Pat. No. 6,574,626; referred to herein as "Regelman").

Claim 1

Claim 1 calls for a method comprising reading a test file including a plurality of test vectors to be applied to a device; and determining a required memory needed to execute the plurality of test vectors.

With respect to claim 1, the Examiner states:

> As per claim 1, Regelman et al disclose a method comprising:
> Reading a test file including a plurality of test vectors to be applied to a device; and
> Determining a required memory needed to execute the plurality of test vectors. (See col. 2, lines 21-35).
> In the "BACKGROUND" of the specification, Regelman states:
>
> In order to properly test larger memories the tester must be equipped with a significant amount of memory to properly store all of the test vectors that comprise a single test program. The tester must also be faster than the memory it is testing in order to properly characterize and test the timing characteristics of the IC. Historically, memory testers use SRAM for program storage. The SRAM is embedded into the tester ASIC to achieve the greatest tester efficiency. SRAM is useful because it exhibits a minimum latency permitting accurate reproduction of timing conditions for testing purposes. SRAM, however, is costly. As tests programs increase in size, a natural solution is to merely increase the amount of embedded SRAM in order to accommodate the entire test program.
>
> Regelman, col.2, lines 21-35

Applicant cannot find any disclosure in the above teaching that "the required memory needed to execute [a] plurality of test vectors" should be determined. In fact, applicant cannot even find a disclosure that required memory should be *determined*. Regelman discloses that "the tester must be equipped with a significant amount of memory to properly store all of the test vectors". Regelman also discloses that "a natural solution is to merely increase the amount of embedded SRAM in order to accommodate the entire test program." However, neither of these are ***determining a required memory*** needed ***to execute*** a plurality of test vectors. Accordingly, claim 1 is believed to be allowable.

Claims 2-9 and 16

Claims 2-9 and 16, which each depend directly from independent claim 1, are believed to be allowable for at least the above-identified reasons.

Claims 10-15

Claims 10-15 are rejected for reasons similar to why claims 1-9 are rejected. Applicant therefore believes that claims 10-15 are allowable for reasons similar to why claims 1-9 are believed to be allowable (and also because Regelman does not disclose any sort of "system" with "logic" for executing the steps of Applicant's methods, including ***reading a test file including a plurality of test vectors*** and ***determining a required memory needed to execute the plurality of test vectors***. Accordingly, claims 10-15 are believed to be allowable.

4. Conclusion

In light of the amendments and remarks provided herein, Applicant respectfully requests the timely issuance of a Notice of Allowance.

Respectfully submitted,
Holland & Hart LLP.

James A. Sheridan

By: October 13, 2006

James A .Sheridan
Reg. No. 43,114
Tel: (303) 295-8000